Claims

[c1]   What is claimed is:

1. A method for accessing a memory to protect a memory section from being accessed or changed incorrectly when accessing the memory comprising:

(a) generating a first logic address data;

(b) selectively outputting the first logic address data or a second logic address data as a physical address data by using an address translator according to a control signal; and

(c) accessing the memory according to the physical address data;

wherein the second logic address data is a result obtained after operating the first logic address data.

[c2]   2. The method of claim 1 wherein Step (b) further comprises operating the first logic address data by using the address translator according to a setup value in order to generate the second logic address data.

[c3]   3. The method of claim 2 wherein the setup value is a value representing a characteristic of the memory section.

[c4]   4. The method of claim 2 wherein the setup value is stored in a register.

[c5]   5. The method of claim 2 wherein the address translator further comprises an operating unit, and Step (b) further comprises operating the first logic address data by using the operating unit according to the setup value to generate the second logic address data.

[c6]   6. The method of claim 2 wherein the address translator further comprises a multiplexer, and Step (b) further comprises multiplexing the first logic address data and the second logic address data by using the multiplexer to selectively output the first logic address data or the second logic address data.

[c7]   7. A microprocessor system for accessing a memory comprising:
        a microprocessor for providing a first logic address data;
        a memory comprising a first memory section and a second memory section; and
        an address translator coupled between the microprocessor and the memory to selectively output the first logic address data or a second logic address data as a physical address data;
        wherein the second logic address data is a result obtained after operating the first logic address data and the

microprocessor accesses data of the first memory section or the second memory section according to the physical address data.

[c8]   8. The device of claim 7 wherein the memory is a non-volatile memory.

[c9]   9. The device of claim 7 wherein the address translator operates the first logic address data according to a setup value to generate the second logic address data.

[c10]   10. The device of claim 9 wherein the setup value is a value representing a characteristic of the first memory section.

[c11]   11. The device of claim 9 wherein the address translator further comprises an operating unit to operate the first logic address data according to the setup value in order to generate the second logic address data.

[c12]   12. The device of claim 9 wherein the address translator further comprises a register for storing the setup value.

[c13]   13. The device of claim 7 wherein the address translator further comprises a multiplexer for multiplexing the first logic address data and the second logic address data in order to selectively output the first logic address data or the second logic address data.